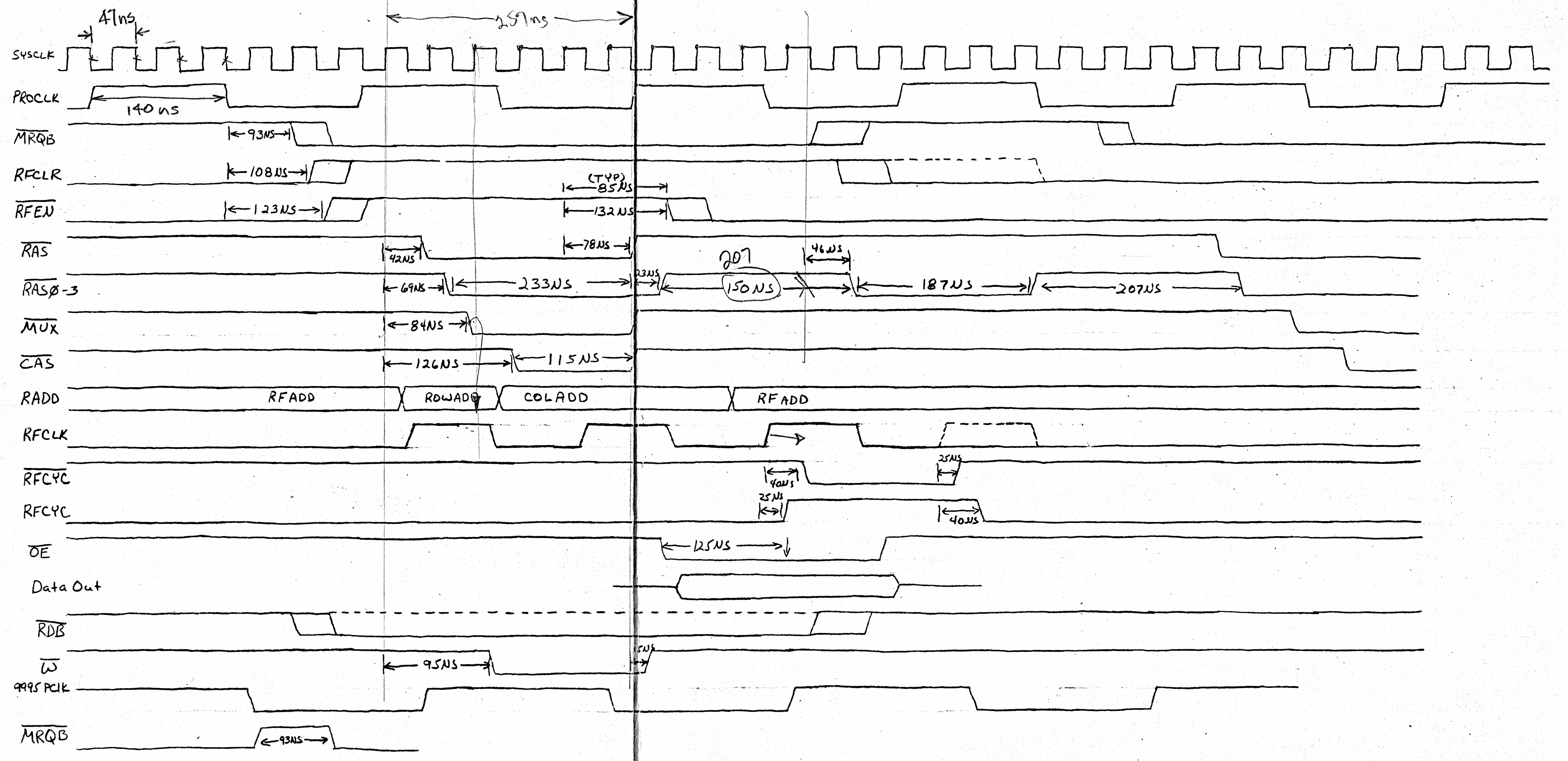
4 3 2 1

D

C

B

A

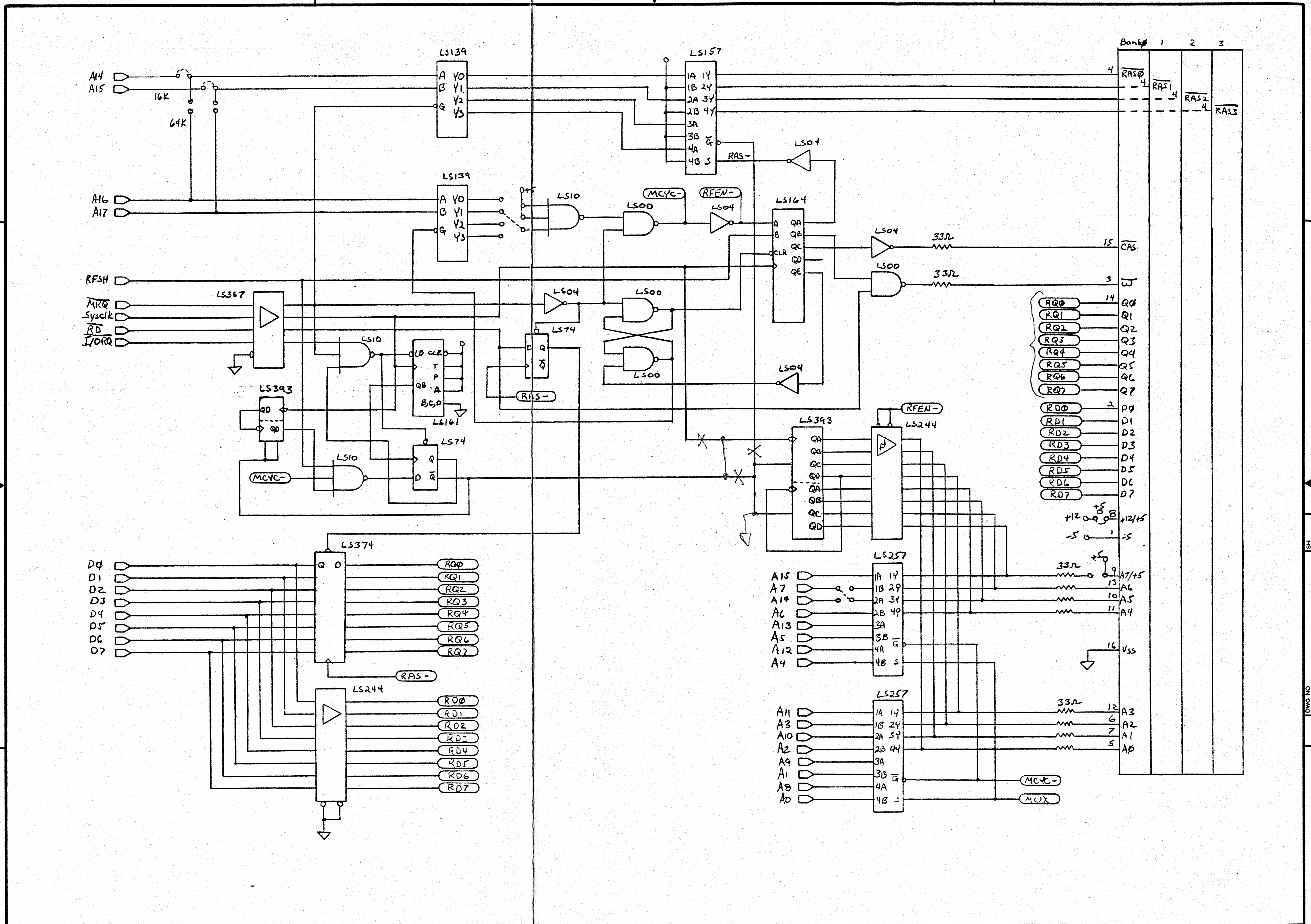

47ns
259ns
SYSCLK
PROCLK
140 ns
$\overline{MRQB}$
93NS
RFCLR
108NS
$\overline{RFEN}$
123NS
(TYP)
85NS
132NS
$\overline{RAS}$
42NS
78NS
$\overline{RAS\emptyset\text{-}3}$
69NS
233NS
23NS
207
150NS
46NS
187NS
207NS
$\overline{MUX}$
84NS
$\overline{CAS}$
126NS
115NS
RADD
RFADD
ROWADD
COLADD
RF ADD
RFCLK
$\overline{RFCYC}$
40NS
25NS
RFCYC
25NS
40NS
$\overline{OE}$
125NS
Data Out
$\overline{RDB}$
$\overline{W}$
95NS
15NS
9995 PCLK
$\overline{MRQB}$
93NS

TEXAS INSTRUMENTS
INCORPORATED
Dallas, Texas

DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
ISSUE DATE		C	96214		
		SCALE		SHEET	

TI-8790C

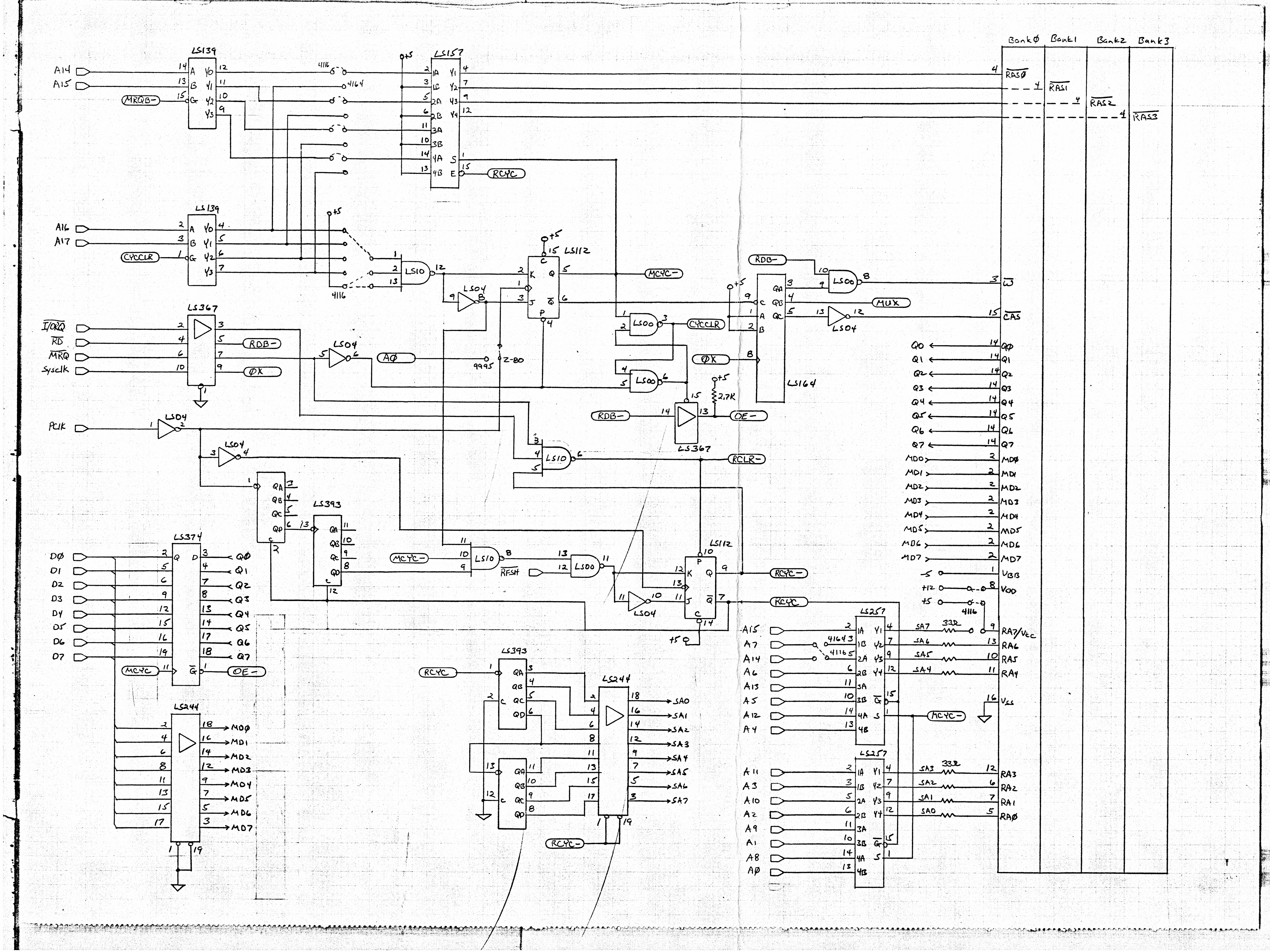
4 3 2 1


D
C
B
A
A14
A15
16K
64K
A16
A17
RFSH
MRQ
Sysclk
RD
I/ORQ
LS139
A Y0
B Y1
G Y2
Y3
LS139
LS367
LS10
LS161
LD CLK
T
P
QB A
B,C,D
LS393
QD
QD
LS10
MCYC-
LS74
D Q
LS157
1A 1Y
1B 2Y
2A 3Y
2B 4Y
3A
3B G
4A
4B S
RAS-
LS04
+5
LS10
LS00
MCYC-
RFEN-
LS04
LS164
A QA
B QB
QC
CLR QD
QE
LS04
LS74
RAS-
LS00
LS00
LS04
LS04
33Ω
LS00
33Ω
LS393
QA
QB
QC
QD
RFEN-
LS244
Bank 0 1 2 3
RAS0
RAS1
RAS2
RAS3
4
15 CAS
3 W
14 Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
RQ0
RQ1
RQ2
RQ3
RQ4
RQ5
RQ6
RQ7
2 D0
D1
D2
D3
D4
D5
D6
D7
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
+12
+5
8
+12/+5
-5
1
-5
33Ω
9 A7/+5
13 A6
10 A5
11 A4
16 Vss
12 A3
6 A2
7 A1
5 A0
LS374
Q D
D0
D1
D2
D3
D4
D5
D6
D7
RQ0
RQ1
RQ2
RQ3
RQ4
RQ5
RQ6
RQ7
RAS-
LS244
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
LS257
A15
A7
A14
A6
A13
A5
A12
A4
1A 1Y
1B 2Y
2A 3Y
2B 4Y
3A
3B G
4A
4B S
LS257
A11
A3
A10
A2
A9
A1
A8
A0
MCYC-
MUX

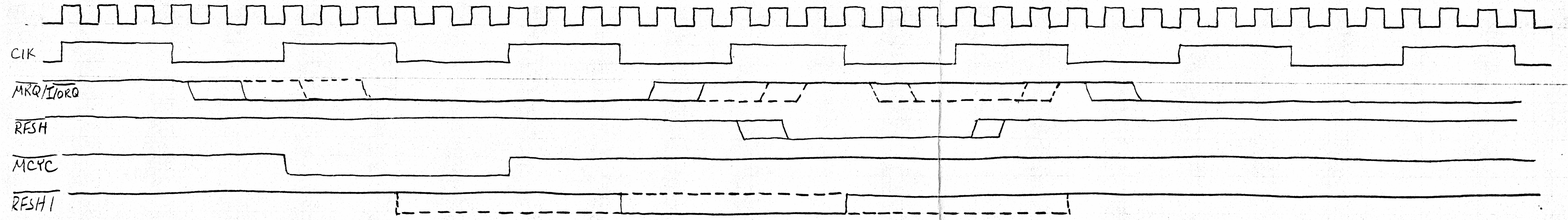
TEXAS INSTRUMENTS
INCORPORATED
Dallas, Texas

DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
ISSUE DATE		C	96214		
		SCALE		SHEET	

T1-8790C

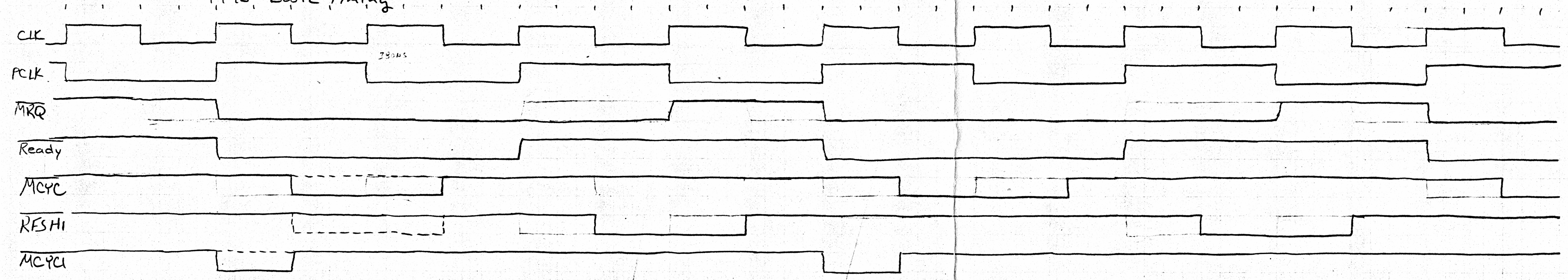


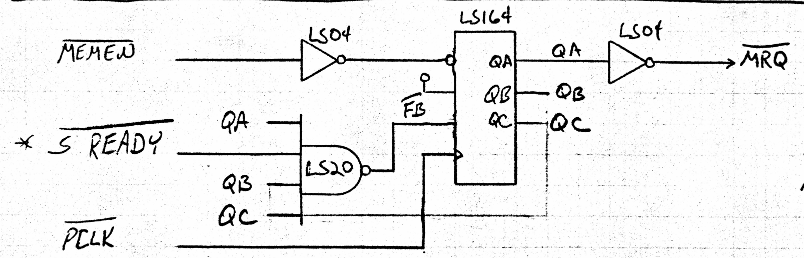
LS139
A14
A15
MRQB-
LS157
4116
4164
+5
RCYC
LS139
A16
A17
CYCCLR
LS10
LS112
LS04
MCYC-
LS00
RDB-
LS00
MUX
LS04
LS164
LS367
I/ORQ
RD
MRQ
Sysclk
RDB-
ØX
AØ
9995
Z-80
ØX
2.7K
RDB-
OE-
LS367
PClk
LS04
LS04
LS10
RCLR-
LS393
LS374
DØ
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
MCYC
OE-
LS10
MCYC-
RFSH
LS00
LS112
LS04
RCYC-
RCYC
LS244
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
LS393
RCYC
LS244
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
RCYC-
Bank Ø
Bank 1
Bank 2
Bank 3
RASØ
RAS1
RAS2
RAS3
W
CAS
-5
+12
+5
4116
VBB
VDD
RA7/Vcc
RA6
RA5
RA4
Vss
RA3
RA2
RA1
RAØ
LS257
A15
A7
A14
A6
A13
A5
A12
A4
41643
41165
33Ω
MCYC-
LS257
A11
A3
A10
A2
A9
A1
A8
AØ
33Ω


ClK
MRQ/I/ORQ
RFSH
MCYC
RFSH1

Z-80 Basic Timing

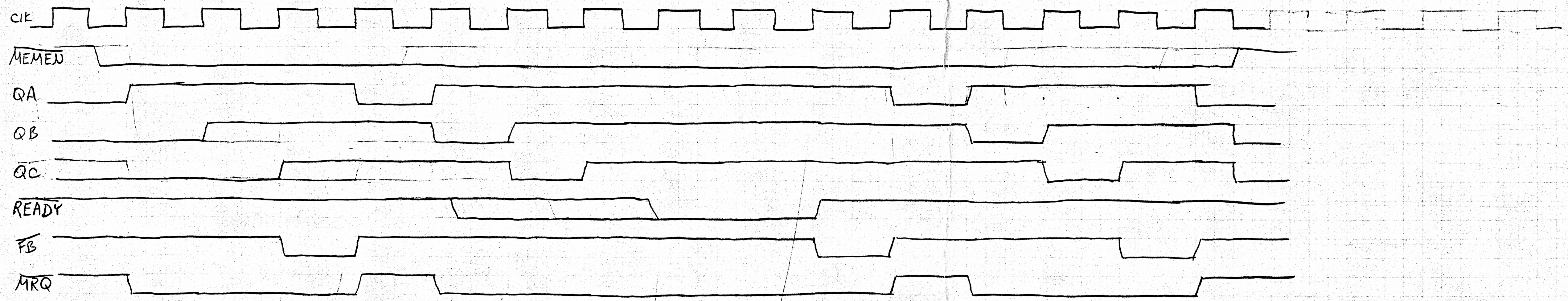
9995 Basic Timing


ClK
PCLK
330ns
MRQ
Ready
MCYC
RFSH1
MCYC1

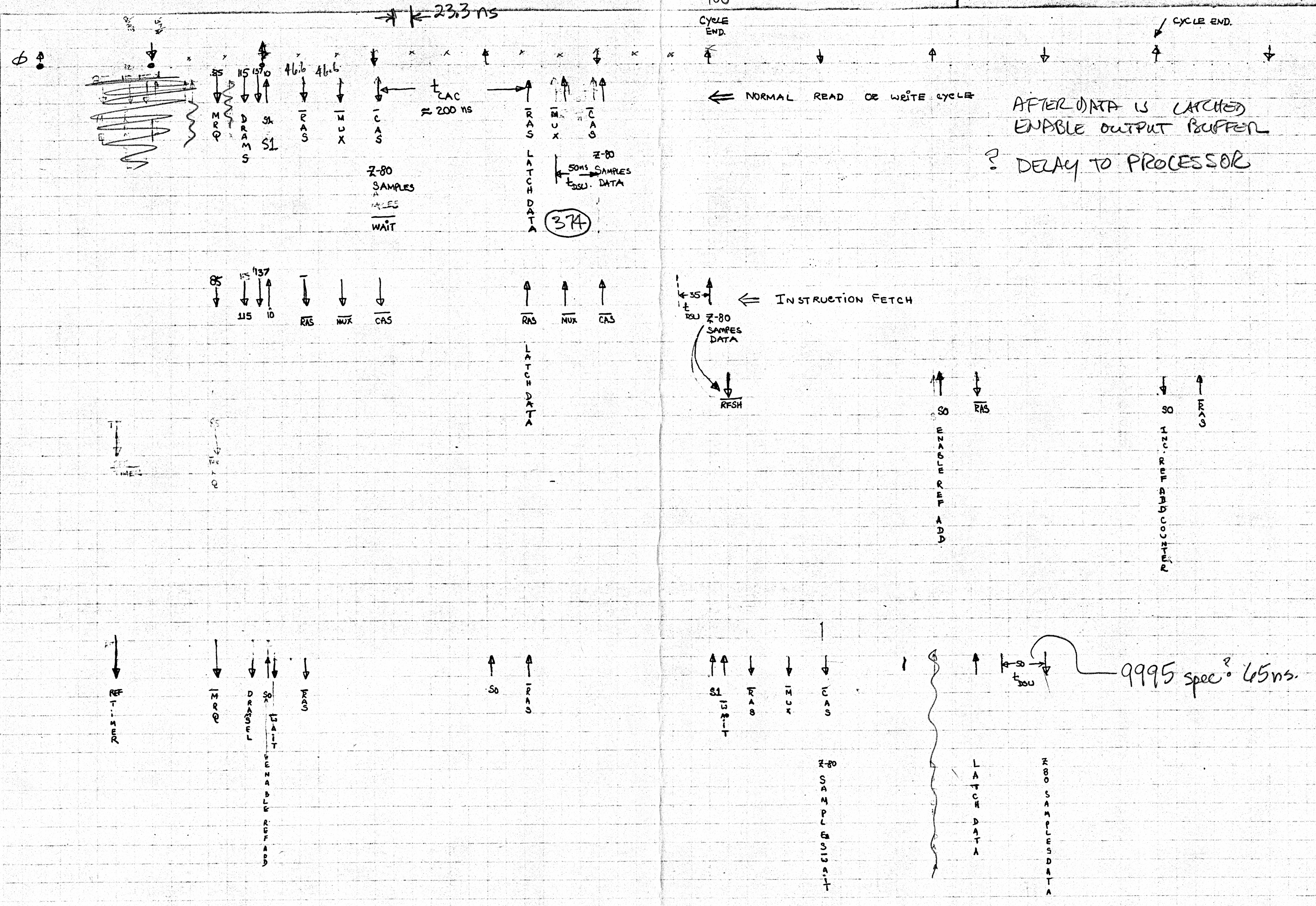

MEMEN
LS04
LS164
QA
QB
QC
QA
LS04
MRQ
FB
* S READY
QA
QB
QC
LS20
PCLK

MRQ Cycle Generation

* Ready Synced with PCLK


ClK
MEMEN
QA
QB
QC
READY
FB
MRQ

700


23.3 ns
CYCLE END.
CYCLE END.
ϕ
85
115
137
10
46.6
46.6
MRQ
DRAMS
S1
S1
RAS
MUX
CAS
t_{CAC}
≈ 200 ns
Z-80 SAMPLES WAIT
RAS
MUX
CAS
LATCH DATA
374
50ns
t_{DSU}
Z-80 SAMPLES DATA
85
115
137
115
10
RAS
MUX
CAS
RAS
MUX
CAS
LATCH DATA
35
t_{DSU}
Z-80 SAMPES DATA
RFSH
SO
RAS
ENABLE REF ADD
SO
RAS
INC. REF ADD COUNTER
REF TIMER
MRQ
DRAMSEL
SO
WAIT
ENABLE REF ADD
RAS
SO
RAS
S1
WAIT
RAS
MUX
CAS
Z-80 SAMPLES WAIT
LATCH DATA
50
t_{DSU}
Z80 SAMPLES DATA

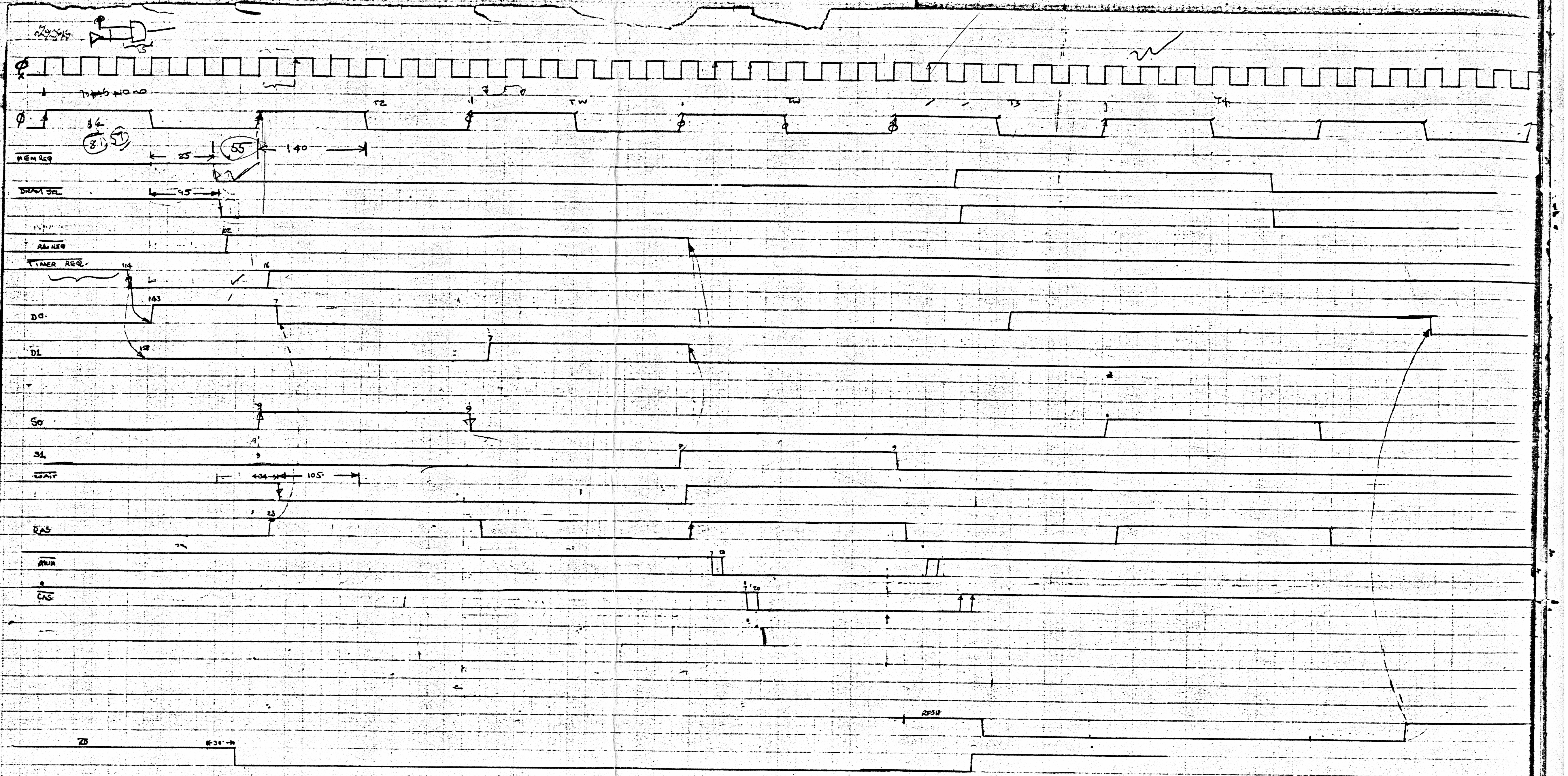
⇐ NORMAL READ OR WRITE CYCLE

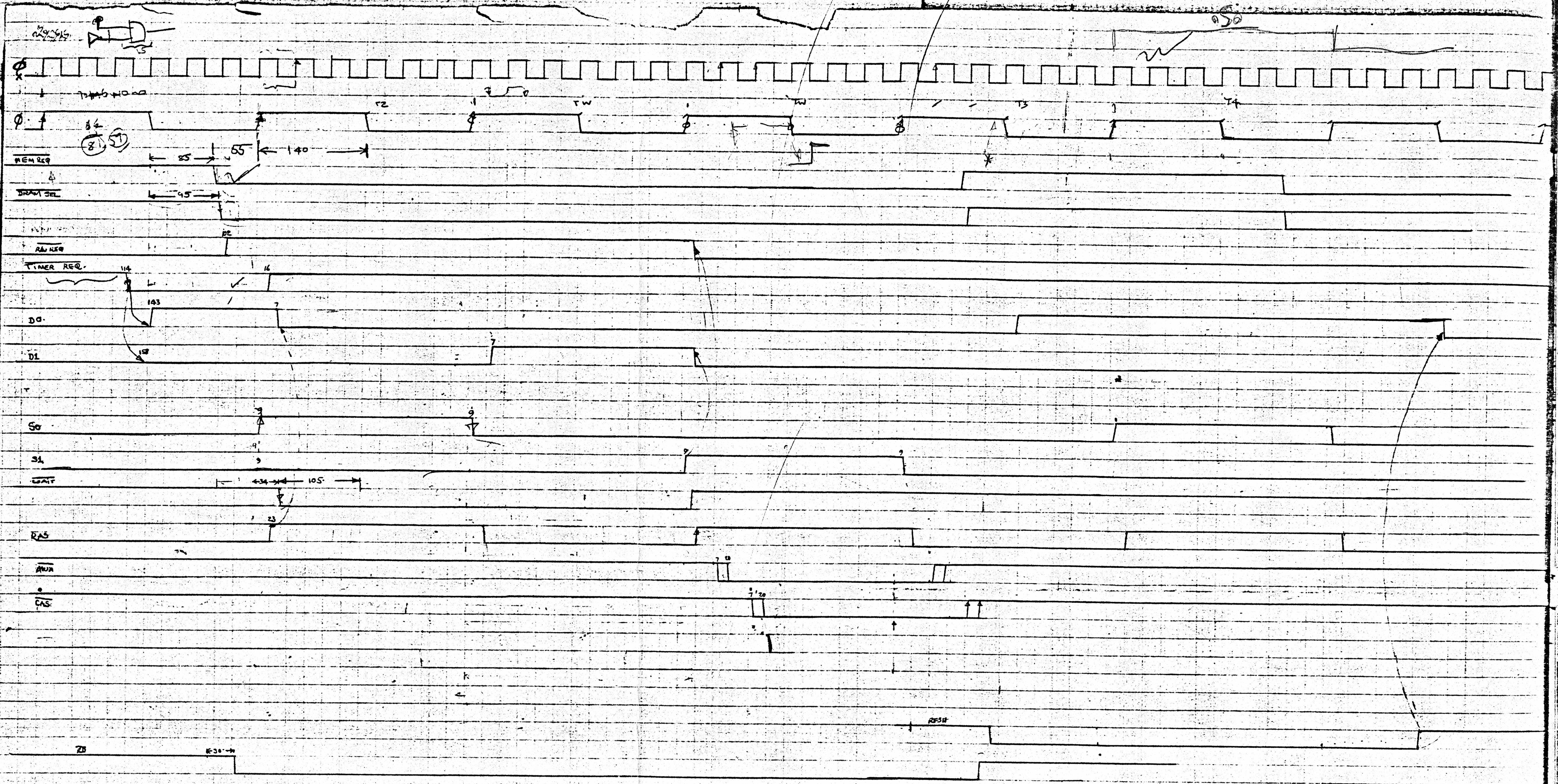
AFTER DATA IS LATCHED
ENABLE OUTPUT BUFFER

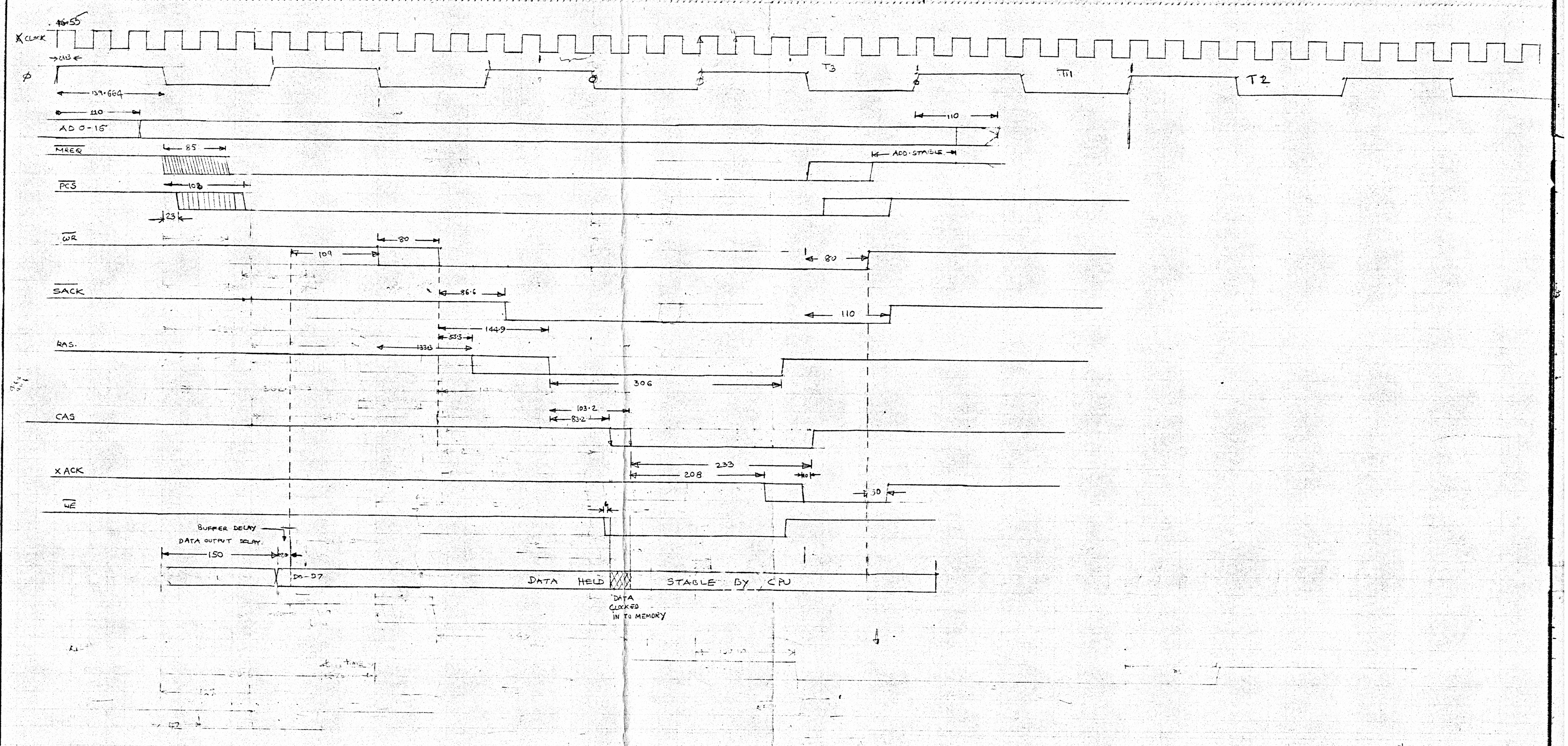
? DELAY TO PROCESSOR

⇐ INSTRUCTION FETCH

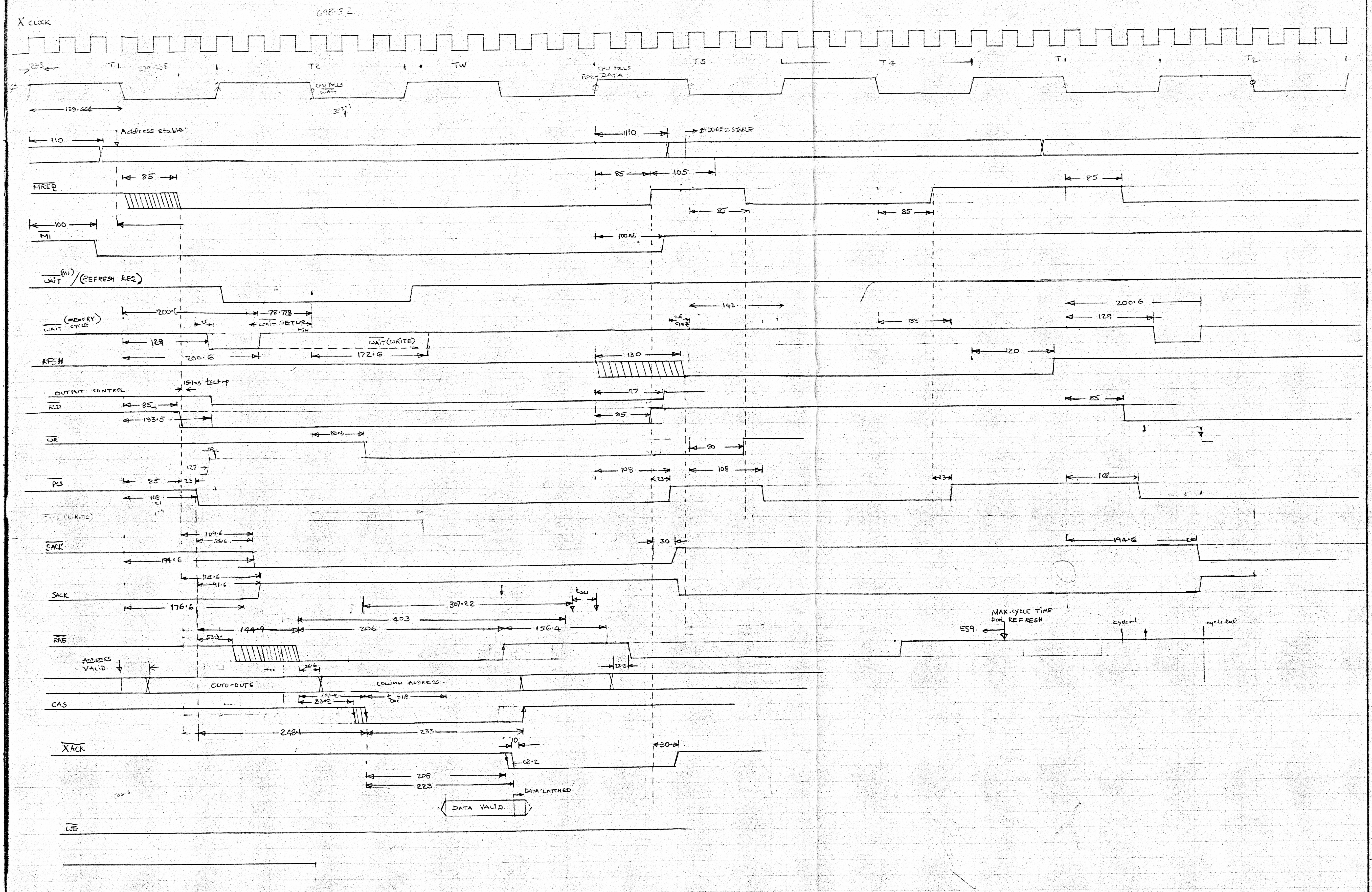
9995 spec? 65ns.

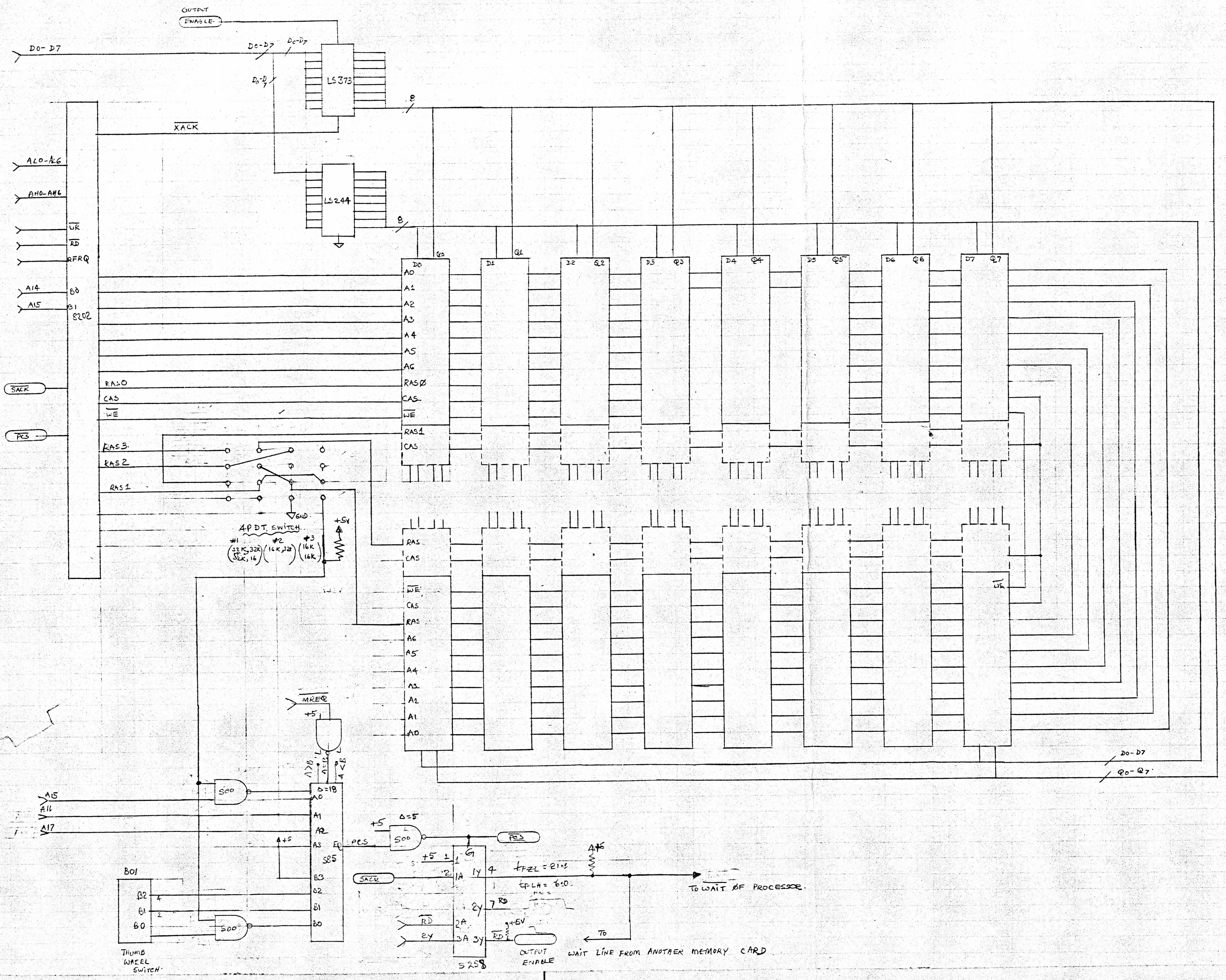

φ
φ
T2
TW
TW
T3
T4
MEM REQ
DRAM SEL
RAM REQ
TIMER REQ.
D0.
D1
S0
S1
WAIT
RAS
MUX
CAS
ZD
84
81
57
55
25
140
45
114
16
143
7
158
9
34
105
23
20
RESET
30

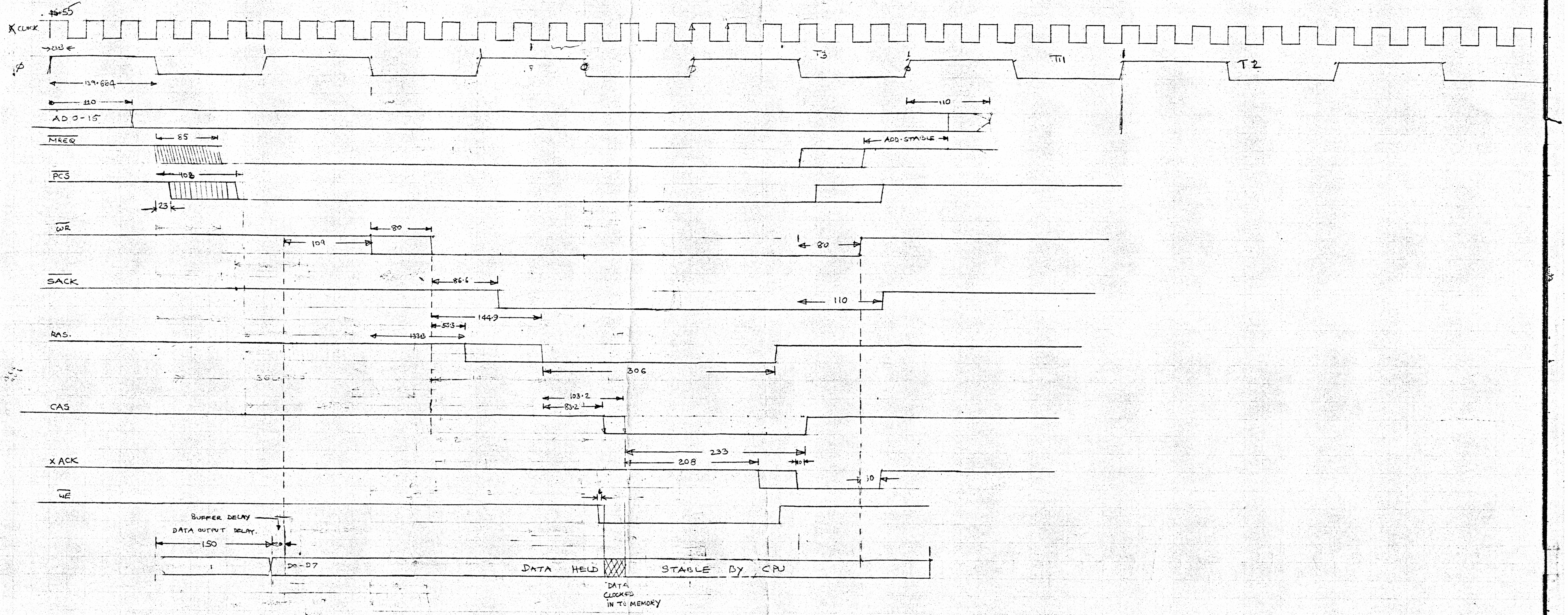

$\overline{\phi}_x$
ϕ
T2
TW
TW
T3
T4
(81)
(57)
85
55
140
95
$\overline{MEMREQ}$
$\overline{DRAM\ SEL}$
$\overline{RAMREQ}$
$\overline{TIMER\ REQ}$
114
16
143
D0
7
D1
158
S0
9
S1
9
$\overline{WAIT}$
34
105
23
$\overline{RAS}$
$\overline{MUX}$
$\overline{CAS}$
20
REFSH
ZB
30

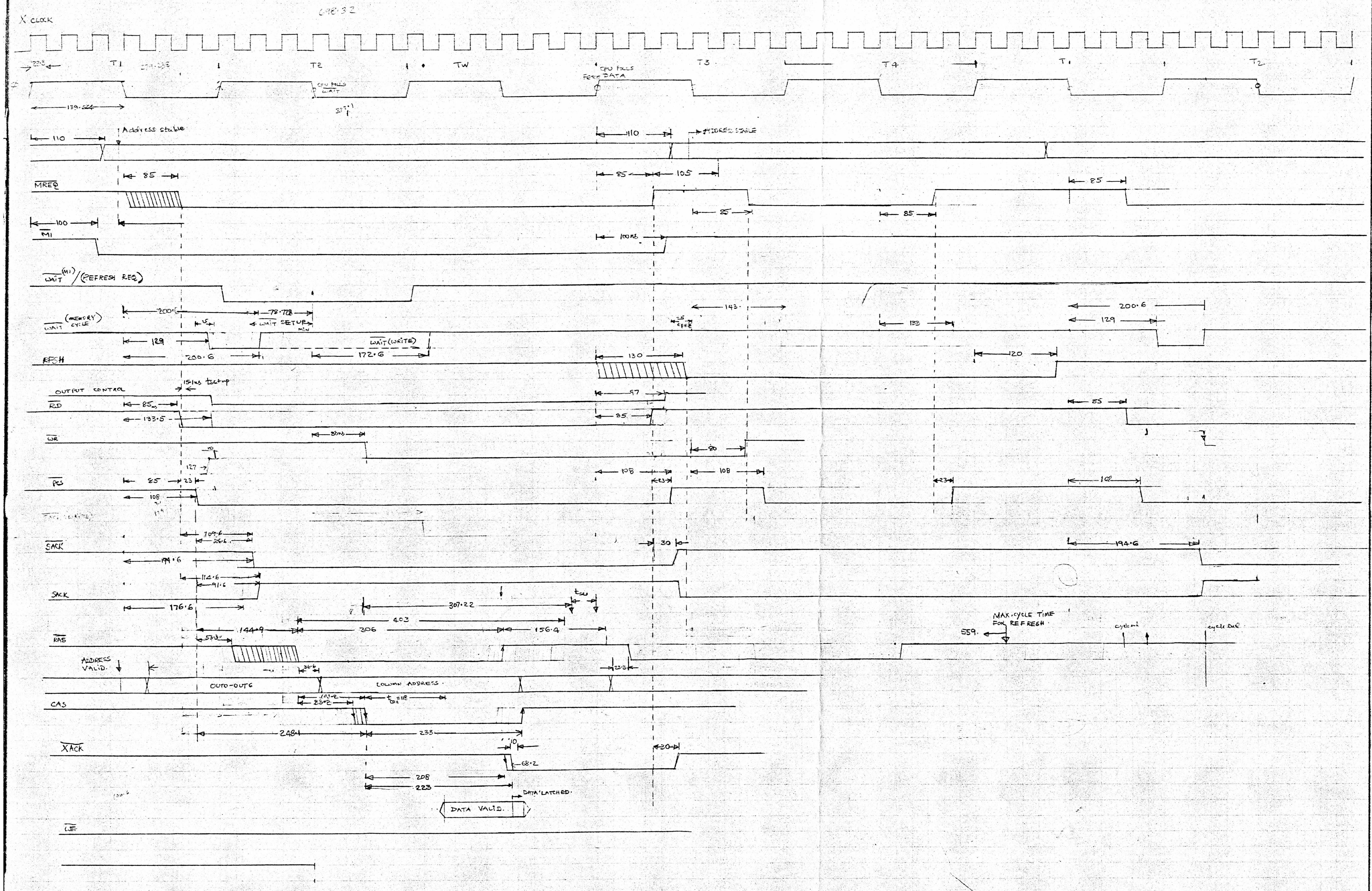


55
X CLOCK
213
ϕ
139·664
T3
T1
T2
110
AD 0-15
MREQ
85
ADD·STABLE
PCS
108
23
WR
109
80
80
SACK
86·6
110
144·9
53·5
133·3
RAS.
306
CAS
103·2
83·2
233
208
10
X ACK
30
WE
BUFFER DELAY
DATA OUTPUT DELAY
150
20
D0-D7
DATA HELD STABLE BY CPU
DATA CLOCKED IN TO MEMORY

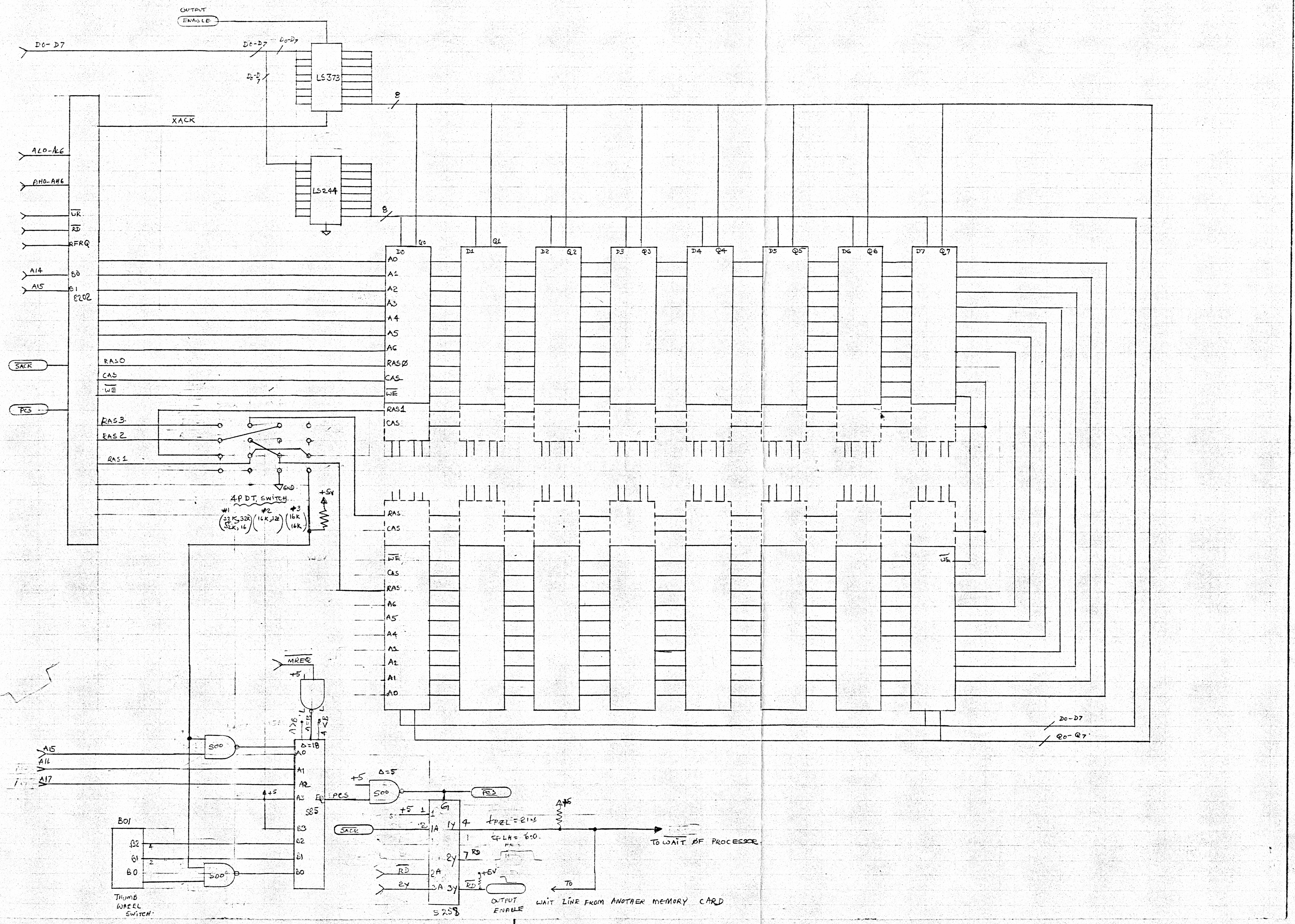

698·32
X CLOCK
T1
T2
TW
T3
T4
T1
T2
CPU POLLS WAIT
CPU POLLS FOR DATA
139·664
110
Address stable
ADDRESS STABLE
MREQ
85
105
M1
100
100ns
WAIT (M1)/(REFRESH REQ)
WAIT (MEMORY CYCLE)
200·6
78·728
WAIT SETUP min
129
143
133
120
RFSH
130
172·6
WAIT (WRITE)
OUTPUT CONTROL
15ns tsetup
RD
133·5
97
WR
80ns
80
PCS
108
23
127
SACK
30
194·6
109·6
114·6
91·6
176·6
307·22
tsu
403
144·9
306
156·4
53·3
MAX. CYCLE TIME FOR REFRESH
559
cycle end
RAS
ADDRESS VALID
ROW-OUTS
COLUMN ADDRESS
23·3
CAS
248·1
233
XACK
10
68·2
208
223
DATA LATCHED
DATA VALID
WE


OUTPUT ENABLE
D0-D7
D0-D7
D0-D7
D0-D7
LS373
8
XACK
AL0-AL6
AH0-AH6
WR
RD
RFRQ
A14
A15
B0
B1
8202
LS244
8
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
A0
A1
A2
A3
A4
A5
A6
RAS0
CAS
WE
RAS1
CAS
SACK
PCS
RAS0
CAS
WE
RAS3
RAS2
RAS1
GND
+5V
4PDT SWITCH
#1 (32K, 32K / 32K, 16)
#2 (16K, 32K)
#3 (16K / 16K)
RAS
CAS
WE
CAS
RAS
A6
A5
A4
A3
A2
A1
A0
WR
D0-D7
Q0-Q7
MREQ
+5
A>B
A=B
A<B
Δ=18
S00
A15
A16
A17
A0
A1
A2
A3
+5
EQ
PCS
S85
B3
B2
B1
B0
+5
Δ=5
S00
PCS
B01
B2
B1
B0
4
2
S00
THUMB WHEEL SWITCH
+5
1
G
SACK
2
1A
1Y
4
tPZL = 21ns
tPLH = 6.0
+5
TO WAIT OF PROCESSOR
2Y
7
RD
RD
2A
2Y
3A
3Y
+5V
RD
OUTPUT ENABLE
S258
TO
WAIT LINE FROM ANOTHER MEMORY CARD

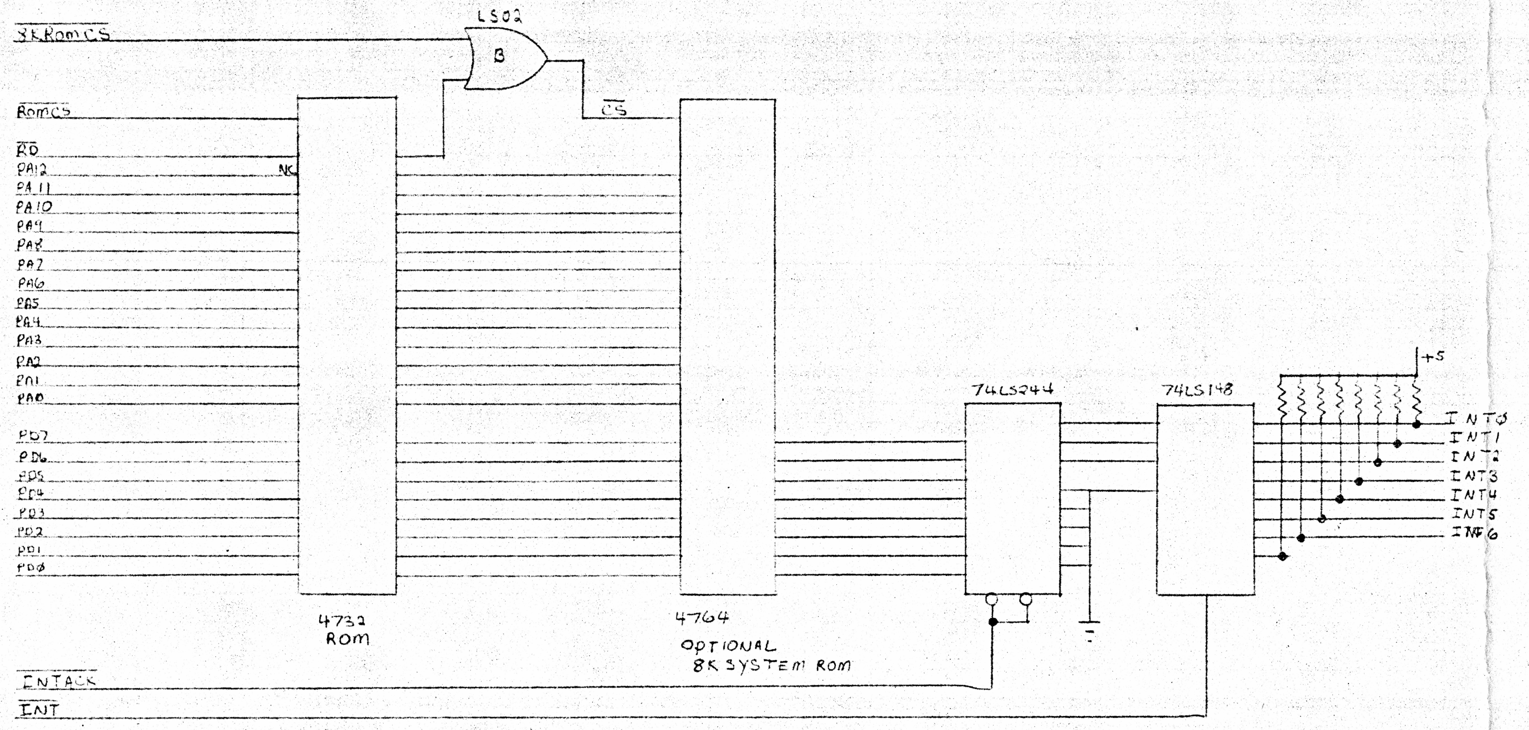

~~16~~ 55
CLOCK
23.3
Ø
139.664
110
AD 0-15
MREQ
85
PCS
408
23
WR
109
80
SACK
86.6
144.9
53.3
133.8
RAS.
306
103.2
83.2
CAS
233
208
10
XACK
WE
6
BUFFER DELAY
DATA OUTPUT DELAY.
150
20
D0-D7
DATA HELD
DATA CLOCKED IN TO MEMORY
STABLE BY CPU
T3
T11
T2
110
ADD. STABLE
80
110
10


698·32
X CLOCK
T1
T2
TW
T3
T4
T1
T2
139·224
CPU POLLS WAIT
CPU POLLS FETCH DATA
110
Address stable
ADDRESS STABLE
105
MREQ
85
100
M1
100NS
WAIT (M1) / (REFRESH REQ)
WAIT (MEMORY CYCLE)
200·6
78·728
WAIT SETUP MIN
129
WAIT (WRITE)
172·6
143
133
RFSH
130
120
OUTPUT CONTROL
15ns tsetup
RD
133·5
97
WR
80ns
80
127
PCS
108
23
SACK
109·6
86·6
194·6
30
SACK
114·6
91·6
176·6
307·22
tsu
403
144·9
306
156·4
53·3
RAS
MAX. CYCLE TIME FOR REFRESH
559.
cycle end
cycle end
ADDRESS VALID.
36·6
23·3
OUTO-OUT6
COLUMN ADDRESS
CAS
103·2
23·2
tCAC=118
248·1
233
XACK
10
68·2
208
223
DATA LATCHED.
DATA VALID.
WE

Z-80


OUTPUT ENABLE
D0-D7
D0-D7
D0-D7
D0-D7
LS373
8
XACK
AL0-AL6
AH0-AH6
WR
RD
RFRQ
A14
A15
B0
B1
8202
LS244
8
SACK
PCS
RAS0
CAS
WE
RAS3
RAS2
RAS1
GND
+5V
4PDT SWITCH
#1 (32K, 32K, 32K, 16)
#2 (16K, 32K)
#3 (16K, 16K)
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
A0
A1
A2
A3
A4
A5
A6
RAS0
CAS
WE
RAS1
CAS
RAS
CAS
WE
CAS
RAS
A6
A5
A4
A3
A2
A1
A0
WE
D0-D7
Q0-Q7
MREQ
+5
A>B
A=B
A<B
Δ=18
S00
S00
A15
A16
A17
A0
A1
A2
A3
EQ
+5
B3
B2
B1
B0
585
B01
B2
B1
B0
THUMB WHEEL SWITCH
+5
Δ=5
S00
PCS
PCS
G
+5
1
2
1A
1Y
4
SACK
tPZL = 21ns
tPLH = 6.0
+5
TO WAIT OF PROCESSOR
2Y
7
RD
RD
2A
2Y
3A
3Y
RD
+5V
OUTPUT ENABLE
TO
WAIT LINE FROM ANOTHER MEMORY CARD
S258

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED



8KRomCS
LS02
B
RomCS
RD
PA12
NC
PA11
PA10
PA9
PA8
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PDØ
CS
4732
ROM
4764
OPTIONAL
8K SYSTEM ROM
74LS244
74LS148
+5
INT0
INT1
INT2
INT3
INT4
INT5
INT6
INTACK
INT

99/3B ROM + PRIORITY INT

-2	-1	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REMARKS
QTY REQD					

PARTS LIST

NEXT ASSY | PRODUCT
APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES
  ANGLES ±
  3 PLACE DECIMALS ±
  2 PLACE DECIMALS ±
- DIMENSIONING IN ACCORDANCE WITH ANSI Y14.5

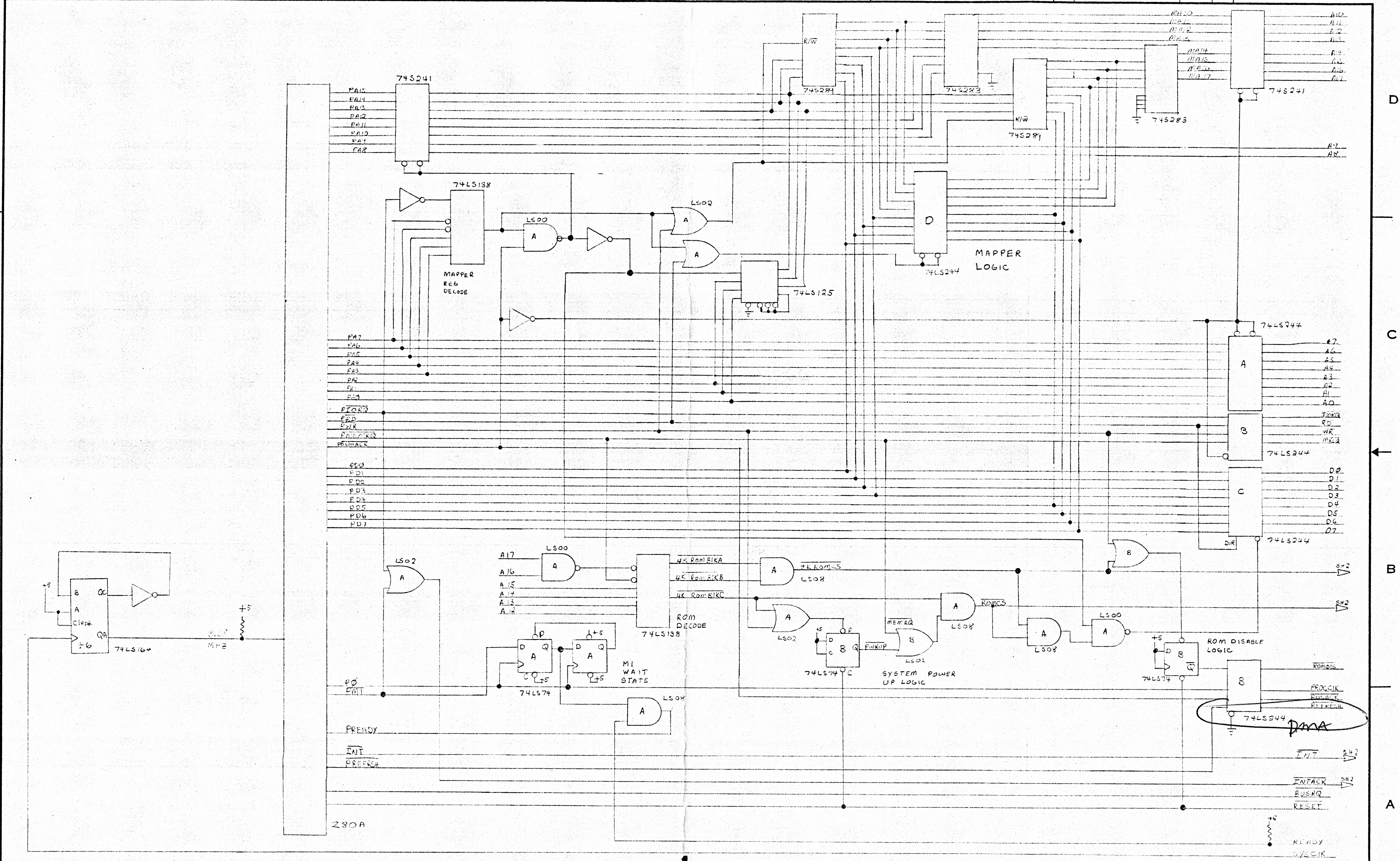
MATERIAL:

DWN
DATE
CHK
DESIGNER
QA
APVD
PRODUCT ENG
DESIGN ACTIVITY RELEASE

TEXAS INSTRUMENTS
INCORPORATED
CALCULATOR PRODUCTS DIVISION

SUP DWG
SIZE D
DRAWING NO
SCALE
REV LTR:
SHEET

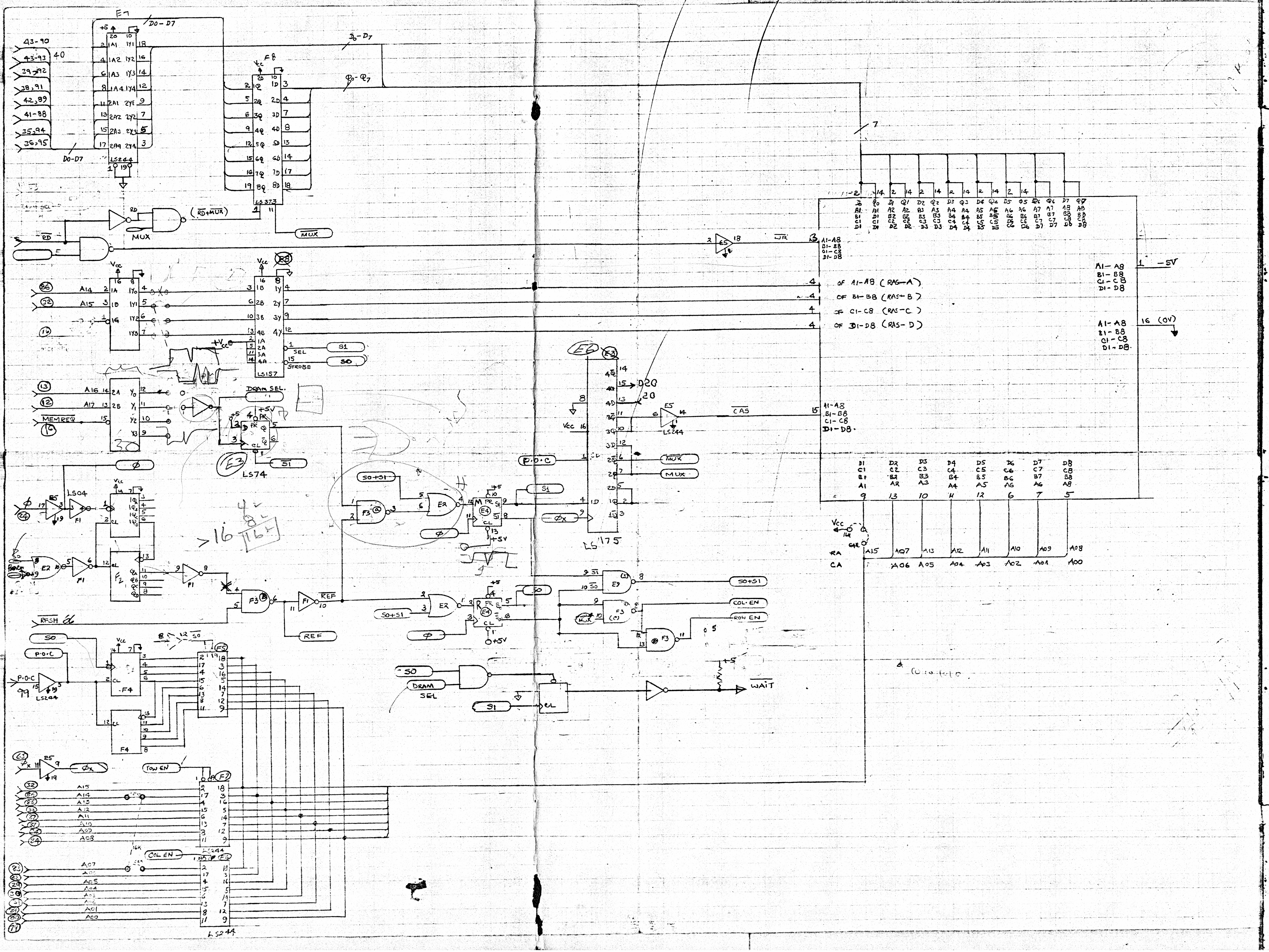
CLASS CODE:


DWG NO
SH
8
7
6
5
4
3
2
1
D
C
B
A
74S241
PA15
PA14
PA13
PA12
PA11
PA10
PA9
PA8
74S289
R/W
74S283
MA10
MA11
MA12
MA13
MA14
MA15
MA16
MA17
A10
A11
A12
A13
A14
A15
A16
A17
A9
A8
74LS138
MAPPER
REG
DECODE
LS00
LS02
74LS125
D
74LS244
MAPPER
LOGIC
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
PIORQ
PRD
PWR
PMEMRQ
PBUSACK
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
A7
A6
A5
A4
A3
A2
A1
A0
IORQ
RD
WR
MREQ
D0
D1
D2
D3
D4
D5
D6
D7
DIR
+5
B
A
Clear
QC
QA
÷6
74LS164
+5
8 MHZ
LS02
A17
A16
A15
A14
A13
A12
4K Rom BlKA
4K Rom BlKB
4K Rom BlKC
ROM
DECODE
74LS138
8K ROMCS
LS08
LS02
8
Q
PWRUP
MEMRQ
LS02
ROMCS
LS08
SYSTEM POWER
UP LOGIC
74LS74
LS00
ROM DISABLE
LOGIC
74LS74
SH2
ROMDIS
PROCCLK
BUSACK
REFRESH
74LS244
DMA
P0
CM1
74LS74
M1
WAIT
STATE
LS08
PREADY
INT
PREFRSH
Z80A
INT
INTACK
BUSRQ
RESET
READY
SYSCLK

99/3B Z80 CPU CARD

TEXAS INSTRUMENTS
INCORPORATED
Dallas, Texas

DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
JTH	09-01-80	D	96214		
ISSUE DATE		SCALE		SHEET	



E7
D0-D7
LS244
F8
D0-D7
Q0-Q7
LS373
7
(RD+MUX)
MUX
RD
E5
WR
LS157
SEL
STROBE
S1
S0
A14
A15
A16
A17
MEMREQ
DRAM SEL.
+5V
E3
LS74
S1
Ø
LS04
F1
E2
F2
F3
REF
RFSH 66
S0+S1
E4
P.O.C
LS244
F4
F5
F7
ØX
ROW EN
COL EN
A15
A14
A13
A12
A11
A10
A09
A08
A07
A06
A05
A04
A03
A02
A01
A00
E6
LS175
D20
MUX
CAS
A1-A8
B1-B8
C1-C8
D1-D8
of A1-A8 (RAS-A)
of B1-B8 (RAS-B)
of C1-C8 (RAS-C)
of D1-D8 (RAS-D)
-5V
16 (0V)
E9
COL. EN
ROW EN
S0
DRAM SEL
S1
CL
WAIT
RA
CA
Vcc

		-20	-25		A	+/-			B	+/-
1	Cycle time	375	410		480				420 → 383 → 336	
2	tw (CH)	80	100		OK				OK	
3	tw (CL) 100	135	165		233				* 115	+
4	tw (RH)	120	150		187				207	
5	tw (RL) 150	200	250		306				* 187	
6	tw (w)	55	75		233				177	
7	tsu (Ac)	-10	-10		OK				OK	
8	tsu (AR)	0	0		OK				OK	
9	tsu (D)	0	0		OK					
10	tsu (WCH)	80	100		233+				146	
11	tsu (WRH)	80	100		233				169	
12	th (ACL)	55	75		220				OK	
13	th (AR) 20	25	35		* 37				* 1.5?/18	233
14	th (ARL)	120	160		327				280	
15	th (CRL)	200	250		327+				* 200	
16	th (DCL)	55	75		233+					
17	th (DRL)	120	160		327+					
18	th (DWL)	55	75		233+					
19	th (RD)	0	0		233+					
20	th (WCL)	55	75		190				130	
21	th (WRL)	120	160		300				230	
22	t (CHRH) 100	135	165		* 165?	⑱⓪ 180			* 138	
23	t (CHRL)	-20	-20		OK				230	
24	t (RLCL)	25	35		83				84	
25	t (WLCL)	-20	-20		0				95	
26	ta (C)	135	165		223					
27	ta (R)	200	250		326					
28										

OPERATING UNIT: PREPARED BY: DATE:

UNIVERSAL PLANNING FORM

TI-9470B